COMPUTE

the Club Of Microprocessor Programmers, Users, and Technical Experts

Georgia Marszalek, Editor • David Graves, Editor

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An IMP-16 Microcomputer System-Part 3 by Hal Chamberlin

First here are some news items. Two more 4K RAM's have been qualified for use in the PUNIBUS system. The Signetics 2604 and the National Semiconductor MM5280-5 or better have been found to work well with wide operating margins. When mixing the various 4K RAM types on the same memory board it should be noted that the TMS4030 requires −3 volts for Vbb whereas the others required −5. Although changing a simple zener diode on the memory board will accommodate the different voltages, 4030's cannot be mixed with the others on the same board.

Fred Holmes (101 Brookbend Ct., Maudlin, SC 29662) is starting a hobbyist oriented user's group and has available supporting documentation on this project such as a cross reference of parts and suppliers. They have a system going (took only two days to get the CPU and 8K of memory operational after construction) and have developed some basic level software such as model 15 teletype output and TCH cassette read/write.

Items presently available from the author are as follows: 8K by 16 memory board $31.00 postpaid, Wire-wrap board for CPU and interface construction $26 PPd, motherboard for 6 100 pin edge sockets $24.00 PPd, raw extender board without edge socket, $15 PPd. All boards except the extender are plated thorough with gold-plated edge fingers. The blueprint packet for $4.00 also includes foil patterns for these boards. Delivery on the above items is 1 to 6 weeks depending on the supply of boards, and orders should be addressed to: Hal Chamberlin, 29 Mead Street, Manchester, New Hampshire 03104. One of our active IMP-16 enthusiasts in Germany is presently laying out a CPU board but it will still be a couple of months before he will be finished. The limited supply of slow $7.50 4K RAM's is exhausted but finally a hobbyist supplier now has full spec 2107B's at a reasonable price. The place is: Integrated Electronics, 5100 El Camino Real, Los Altos, CA 94022 and the price is $8.00. They also have 8833's for $1.65.

In this installment we will finish up the discussion of the CPU board. The first two pages of CPU drawings were published in *COMPUTE* Vol. 2, No. 7. A couple of minor errors have been found by readers. On the timing generator drawing, inversion bars should be added to RAW DATA OUT ENAB and to 01,03, 05, and 07. Also there is an error in the address sequence timing ROM contents listing. The output named CPU DATA IN ENAB in the CPU-2 ROM should have ONES at address 20 and 28. The time sequence listing is correct. Those who ordered blueprints before March 1 should check the remainder of the CPU drawings in this issue for other similar errors which have been corrected.

Connection of the 5 or 6 IMP-16 chips to the PUNIBUS involves two kinds of interface considerations. The first is the signal routing and logic level interface and the second is the timing relationship interface. In addition, the IMP chips require some additional external logic not directly related to the bus interface.

The IMP-16 is a microprogrammed chip set with the microprogram stored in a portion of the CROM (Control Read-Only Memory) chip. A standard system would have one CROM but the circuitry necessary to accept an additional CROM is provided on the CPU board. The additional CROM may be either the "extended CROM" or the "power math CROM", both implementing enhanced arithmetic instructions. Due to the fact that memory mapped I/O is used with the PUNIBUS, the "power I/O CROM" will be of limited use although its other functions will work OK. It could have been made much better if a block move instruction was included along with the memory search instructions. The CROM controls the operation of 4 RALU (Register and Arithmetic Logic Unit) chips directly over 4 "control bus" lines and 2 "carry/shift" lines and indirectly through "control flags".

When −12 volt power and the 4-phase clocks are applied, the CROM continuously fetches and executes micro-instructions at a 714 kHz rate or one every 1400 Ns (2 bus cycles). All microcycles are essentially the same; differences are in the data patterns sent and received by the CROM over the various busses. The following will be a brief description of microprocessor operation. For greater detail the reader is referred to National Semiconductor publications on the IMP-16.

The internal structure of the RALU is diagrammed in figure 1. Basically it is a classic three bus register file and arithmetic-logic unit (ALU) architecture. To do an operation, two operands are selected from the register file and put onto the A and B buses. The ALU combines them according to a control code and places the result on the R (result) bus. Fundamentally an operation is completely specified by giving the register addresses of the two source operands, the ALU function code,

and the register address for result storage. Input and output to the external world is handled by an I/O multiplexor on the R bus. For output it can either send the R bus contents or the A bus contents out. For input it can replace the R bus contents with external data.

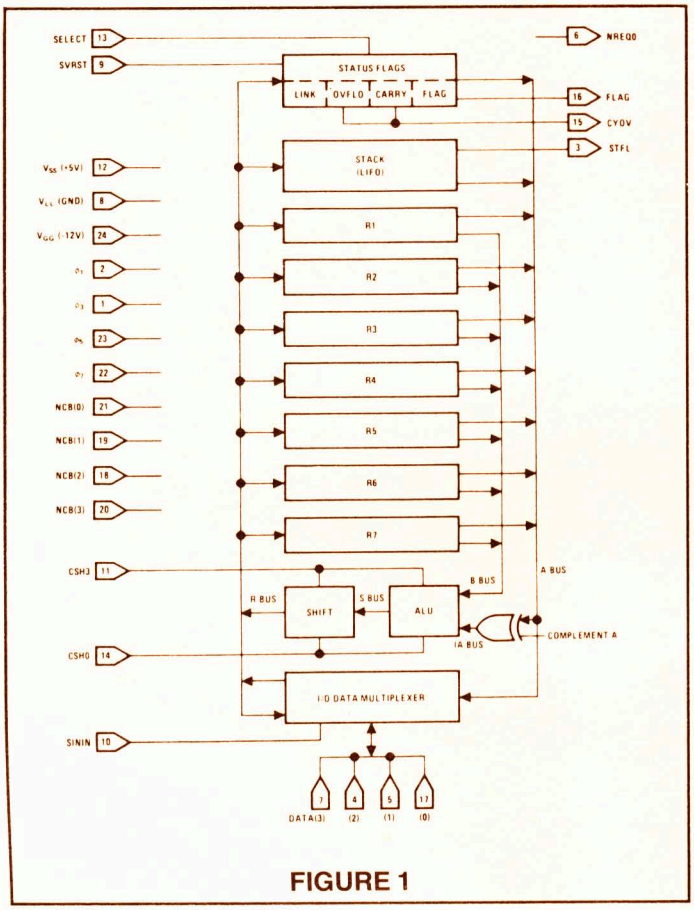


FIGURE 1

Commands to the RALU's from the CROM are sent over 4 "control bus" lines (NCB0-NCB3) in 4 time slices (T1, T3, T5, and T7). Essentially the 4 bit pattern on the control bus during T1 specifies an RALU register to be gated onto the A bus of the RALU and another 4 bit pattern during T3 specifies the source for the B bus. During T5 an ALU function is specified and during T7 the ALU output disposition is specified. Thus a complete ALU/register function can be specified and executed each microcycle. Two additional direct lines between the CROM and the RALU's are HOCSH (High Order Carry SHift) and LOCSH. These transmit and receive carry propagation information during T5 and shift information during T7.

The microprogram stored in the ROM portion of the CROM governs the sequence and contents of commands to the RALU's as a function of the instruction being executed. Detailed knowledge of the microprogram is not necessary in order to build, troubleshoot, or program the system.

Associated with the set of 4 RALU's is a 16 bit bi-directional data bus. Data into and out of the RALU's goes over this bus in time slices also. During T1 the RALU "R bus" is sent out. This data is the result of the ALU operation in the previous microcycle. During T3, the "A bus" data selected by the T1 control bus command is sent out. The RALU data bus is turned around during T7 and accepts input data which may replace the ALU output depending on the T7 command.

The op code portion (most significant 9 bits) of data to and from the rest of the system is accepted by the CROM during T7 of instruction fetch cycles. Due to a lack of package pins, 5 of these bits are time multiplexed with other CROM functions on 5 lines. The remaining 4 are dedicated CROM inputs.

In addition to the control bus and carry/shift lines, the CROM controls and monitors system status through control flags and jump conditions. The control flags are in a separate 16 bit TTL register and should not be confused with the status flags which are on the RALU chips. During T1 of every microcycle the CROM outputs a 4 bit "jump/flag" address. The 4 bits are latched in a TTL register which is connected to the address inputs of a 16 input TTL multiplexor (the jump condition multiplexor) and the address inputs of a 16 bit TTL addressable latch (the control flags register). Thus every microcycle can select one jump condition and one control flag but they must have the same address. By means of the NFLEN output, the CROM can set, reset, pulse, or leave unchanged the selected control flag. Likewise, the CROM can either test or ignore the selected jump condition through the NJCND input. Control flags are used by the microprogram to request memory cycles, distinguish between read and write, enable interrupts, and modify RALU operation. Several of the control flags have no specific function but can be manipulated with the SFLG and PFLG instructions. These are brought out to edge finger pins on the CPU board. Also, the two control flags associated with regular input/output instructions have no function in the PUNIBUS system.

Jump condition multiplexor inputs are tied to various combinations of RALU data bits to detect ZERO, negative, etc.; the interrupt request lines, stack full detect, etc. Three jump conditions that are unused in National Semiconductor implementations are connected to detect additional arithmetic result combinations.

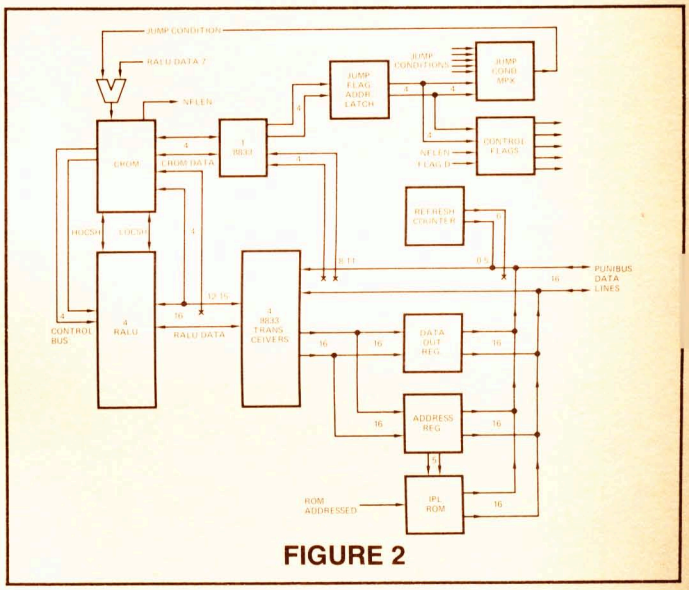


FIGURE 2

The data path interface to the PUNIBUS is diagrammed in figure 2. The main interface is a bus transceiver between the 16 bit RALU data bus and the PUNIBUS. Input data from the PUNIBUS to the CPU passes through the transmitter portion of a set of 8833's onto the RALU data bus. The 4 dedicated CROM inputs are connected directly to bits 12-15 on the RALU data bus. Output data from the CPU is either an address or it is data to be written into memory. Address data comes from the RALU data bus, through the 8833 receivers and into the address register. Memory write data follows the same path but is latched into the data out register. Both of these registers have tri-state outputs which are connected to the PUNIBUS.

Timing control then gates the register contents onto the PUNIBUS at the proper times. The bootstrap loader ROM has tri-state or open-collector outputs which are tied to the PUNIBUS and are enabled whenever the ROM is addressed. The refresh address generator is actually part of the bus controller and is simply tied to the PUNIBUS along with the ROM, data, and address registers.

The lower 8 bits of the address register have separate tri-state drivers. Since these address bits are available throughout a bus cycle, the on-board ROM may be connected to the lower 5 of these bits without a separate ROM address latch. These address register bits are also made available at non-bus pins of the edge connector. The utility of this connection is seen if one looks at the PFLG (Pulse FLaG) instruction description. The lower 8 bits of the instruction word (the CTL field) are latched into the address register prior to the specified control flag being pulsed. This amounts to a sort of "output immediate" instruction which the author has found to be useful in high speed character stroke drawing on a vector graphic display (see The Computer Hobbyst, Vol. 1, No. 3).

Four of the CROM opcode input bits are time multiplexed with the jump/flag address bits. Another 8833 transceiver is used to transmit CROM op-code data from the PUNIBUS to the CROM and to receive jump/flag address data which is sent to the jump/flag address register.

The ninth CROM op-code bit is multiplexed with the jump condition multiplexor output and connected to the NJCND CROM input. Gates were used for the selection because a tri-state output 16 input multiplexor was too difficult to obtain.

The CPU timing interface is relatively simple and is handled entirely by the same ROM timing generator used in the bus controller. No gating of timing signals is required because each microcycle is identical in its timing requirements. Each microcycle is 1.4 microseconds in duration and spans exactly two bus cycles. The bus cycle timing is actually written into the timing ROM twice. Since the same timing generator is used for CPU and bus, the phasing between CPU and bus is fixed.

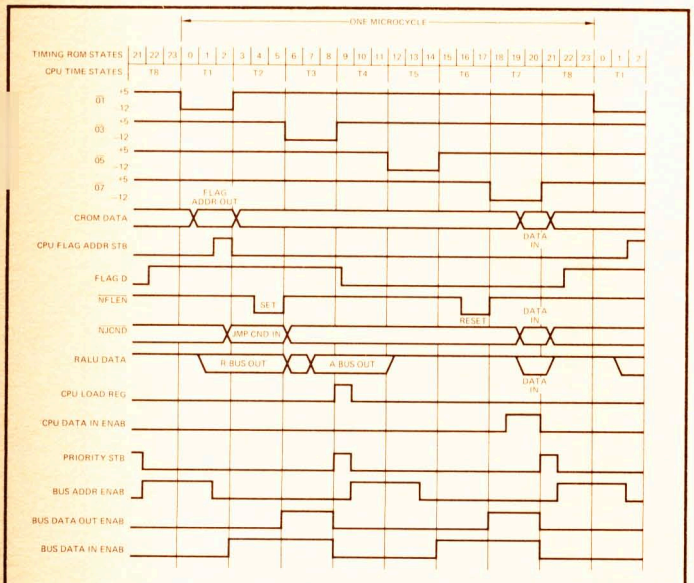


FIGURE 3

Figure 3 shows a timing diagram for the CPU, and for reference purposes, some of the bus timing signals. The most basic CPU timing signals are the 4-phase non-overlapping clocks. These are PMOS logic levels (0=+5, 1=−12) applied to all 5 IMP chips. The odd-numbered CPU states (T1, T3, T5, and T7) occur when the similarly numbered clock phases are active. The dead spaces between clock pulses are assigned to the even numbered CPU states. Each CPU time state is three 58.3 NS bus clock cycles long for a total of 175 NS.

The 4 shared CROM data lines send out the jump/flag address during the latter part of T1 and accept op-code data input at the latter part of T7. The 8833 transceiver connected to these lines is normally selected to receive from the CROM and send to the flag address latch. A one bus clock long pulse at the end of T1 called CPU FLAG ADDR STB causes the jump/flag address to be latched into the flag address latch. When CPU DATA IN ENAB is active during the last two thirds of T7, the transceiver transmits op-code data to the CROM.

As was mentioned before, the CROM may set, reset, pulse, or leave unchanged the addressed control flag by means of the NFLEN signal. The microprogram may selectively cause NFLEN to be active during T2 or T6 or both. If it is active during T2, the addressed control flag will be unconditionally set at this time. If it is active during T6, the addressed flag is unconditionally reset. If NFLEN is active at both T2 and T6, the flag will be turned on at T2 and turned back off at T6. The net result is that the flag will be pulsed if it was initially off or reset if it was initially on. The addressable latches used in the CPU are D-type however rather than set-reset. The proper operation is accomplished in conjunction with the FLAG D timing signal. FLAG D is a logic ONE during T2 and a logic ZERO during T6 and is connected to the latch's D input. NFLEN is then connected to the latch's enable input. Thus if the latch is enabled (clocked) during T2 (NFLEN active) then the addressed bit will be set since the D input (FLAG D) is high. Likewise if it is enabled during T6, the addressed bit will be reset.

The NJCND input to the CROM is shared with the ninth OP-code bit. Like the other 4 shared lines, it is normally set up for its alternate function. When CPU DATA IN ENAB is active it is switched to data in mode.

The 8833 transceivers connected to RALU data are normally set to receive data from the RALU's and send it to the registers and jump condition logic. They are turned around only during CPU DATA IN ENAB time. During the latter part of T1 and all of T2, the result of the last ALU operation appears on the RALU data bus. This is the same time that the jump conditions are sensed. Thus simple combinational logic is all that is required to encode the various jump condition combinations.

Both the data and address registers are clocked every microcycle by the CPU LOAD REG signal. This signal occurs at the beginning of T4, the same time that the "A bus" in the RALU's is being sent out. Whether or not a register is enabled for loading is dependent upon the state of the RDM (ReaD Memory), WRM (WRite Memory), and LDAR (LoaD Address Register) control flags. The address register is loaded if RDM or LDAR is active and the data out register is loaded if WRM is active. Otherwise their contents are left unchanged.

The timing of CPU DATA IN ENAB in the PUNIBUS system is different from that employed by National in their IMP-16C. In the IMP-16C valid data is applied to the CROM and RALU's during the entire T7 state and parts of T6 and T8 as well. However, a look at the MOS chip data sheet reveals that valid data is only necessary within 45 NS of the end of T7 *provided* that the invalid data to the RALU's during the preceding 130 NS of T7 is logic ONE (high). Note that the CROM data inputs do not have this restriction and that the setup time to the end of T7 is only 35 NS. Taking advantage of this fact allows up to 130 NS additional for memory access and bus delays. The

invalid data being ONES requirement is taken care of automatically by the on-chip pull-up transistors and the fact that the 8833 transmitters are not enabled until they have valid data at their inputs. The result is that the pull-up transistors pull the inputs to a high level during T6 and T7 and the 8833's either leave the inputs high for a ONE or pull them down during the latter part of T7 for a ZERO.

The microprogram requests read bus cycles by pulsing the RDM flag and requests write cycles by pulsing WRM. From the timing diagram it can be seen that these flags are turned on at the beginning of T2 and off again at the beginning of T6. The time that they are on perfectly spans BUS PRIORITY STB and BUS ADDR ENAB. Thus tying these flags directly to the bus cycle request logic insures that the single, correct bus cycle needed by the CPU will be requested. Since the CPU is the highest priority bus user, the needed bus cycle will always be granted. Further, since BUS ADDR ENAB is spanned, WRM can be factored into the write cycle request logic directly.

Now, for a moment, look back in *COMPUTE* Vol 2, No. 7 at part 2 figure 3 and locate the clock driver circuitry. It can be seen that the 4-phase non-overlapping clocks are developed by a 1-of-10 decoder connected to three next state address lines on the timing generator. In generating phases 1, 3, 5, and 7, the A and B inputs to the 7442 select the phase and C acts as an enable (see timing ROM truth tables). The D input is used to disable the clocks during system reset. The MH0026 clock drivers are driven through capacitor level shifters by 74S04's which cancel the inverted outputs of the decoder with minimal additional delay. Clock overshoot and ringing at the IMP chips is controlled with 10 ohm series damping resistors. 3.3K resistors to ground establish a minimum load current enabling the clock drivers to absorb any clock cross-coupling.

Figure 4 shows the actual interconnections among the 2 possible CROM's and 4 RALU's. The optional extended CROM is connected in parallel with the standard CROM except for 4 of the op-code input bits. One of these is connected to a 4-input NOR equivalent which detects the extended op-code range and the other three connect to bits not normally used for op-codes in the standard CROM.

An emitter follower buffer is shown in series with the carry/shift line between the middle two RALU's. Except during T7 this circuit acts as an emitter follower and aids driving of the carry line capacitance thus speeding carry propagation during T5. During T7, the collector supply voltage is cut off making the circuit look like two back-to-back diodes. This allows normal shifting operations which may travel in either direction along the carry/shift line. Use of this circuit appears to subtract about 1.5 to 2 volts from the high logic level of the carry signal thus reducing operating margin. However omission of the circuit slows carry propagation such that carry out from the most significant RALU at the end of T5 may be lower yet due to capacitance charging. While the circuit may help the carry signal during T5, it degrades the shift signals, particularly right shifts, during T7. This is by far the most critical part of the CPU. Slow carry propagation is also the most likely cause for rejection of "surplus" IMP chip sets.

Three of the RALU outputs are open drains and require pulldown resistors. Stack full (STFL) and NREQ0 are wire-or lines for detecting a non-zero bottom stack word and non-zero RALU bus contents respectively. The general purpose status flag outputs of the RALU's are latched since they are invalid

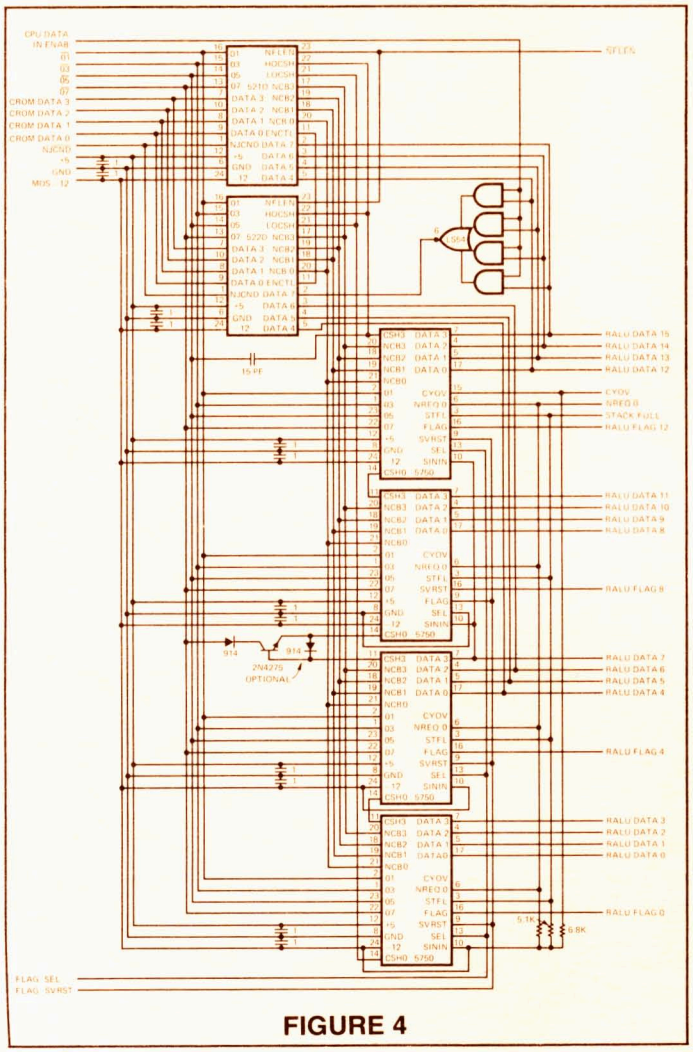


FIGURE 4

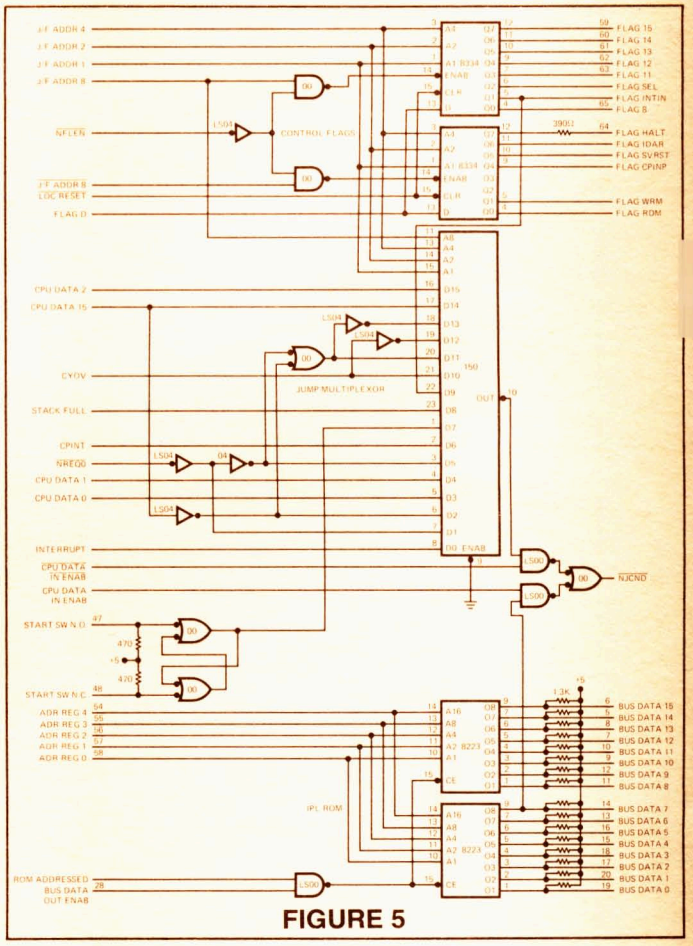


FIGURE 5

during part of each microcycle and made available at non-bus pins of the edge connector.

The control flags and the jump condition multiplexor are shown in figure 5. Some additional gating is necessary on the 8 bit addressable latches to make them look like a single 16 bit addressable latch. The HALT and interrupt enable control flags are routed to edge fingers through series resistors for direct LED connection. The unspecified control flags are also made available at the edge connector. Gating and inverters on the jump condition multiplexor inputs decode the six arithmetic result combinations (+, not +, 0, not 0, −, not −) as well as carry and not carry. Other inputs detect various machine status conditions. The appendix lists the 16 jump condition codes and the condition associated with each. An AND-OR gating array is used to multiplex the NJCND input of the CROM between the jump condition multiplexor output and the least significant op-code bit. The START input to the jump condition multiplexor is debounced by two cross-coupled NAND gates allowing a simple SPDT switch to be connected directly to the edge connector. The HALT instruction simply sends the microprogram into a loop testing the START jump condition. When a ONE is detected, the microprogram resumes fetching and executing macro instructions.

The IPL (Initial Program Load) ROM's are also in figure 5. Their outputs, which are connected directly to the backplane bus, are enabled by the coincidence of ROM ADDRESSED and BUS DATA OUT ENAB. A location within the ROM is directly addressed by the lower 5 bits of the CPU address register. Note that because of this address connection only the CPU can properly address the ROM, DMA devices cannot.

Bus termination resistors are shown connected to the ROM outputs. These serve mainly to pull up the bus data lines to a logic ONE when they are not driven. This prevents the lines

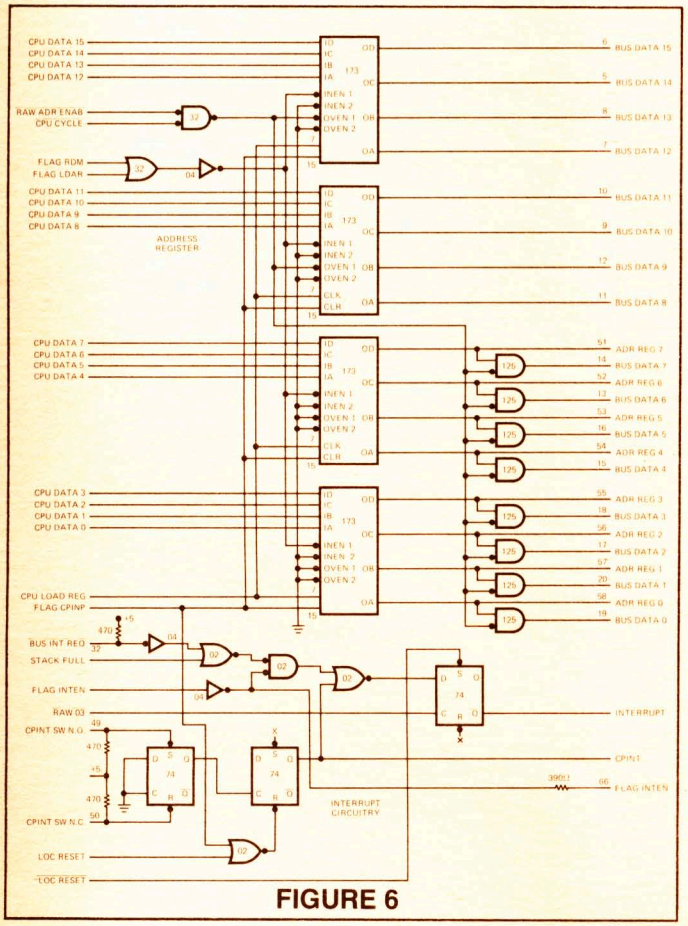


FIGURE 6

from floating around the logic threshold and inducing receiver oscillation. They also allow the use of open collector devices on the bus as well as tri-state devices. These resistors could be placed on the backplane rather than the CPU board if desired. Their value should not be smaller than 1K because of limited drive capability.

Figure 6 shows the address register and interrupt logic. The address register is clocked every microcycle by CPU LOAD REG. Gating enables the address register to be loaded if either the RDM (ReaD Memory) flag or the LDAR (LoaD Address Register) flag is on. The lower 8 bits of the address register have separate tri-state buffers thus giving a static address to the ROM. The tri-state outputs are enabled when CPU cycle and ADDRESS ENAB are coincident.

The two possible general interrupt sources, BUS INT REQ and stack overflow, are first OR'ed together and then AND'ed with interrupt enable which is a control flag. A 7474 flop is used to strobe the resulting interrupt request so that it does not change while the CPU is testing it. Actually, interrupt request is just another jump condition multiplexor input that is tested by the microprogram at the beginning of every instruction fetch sequence. The strobe timing must be chosen carefully so that it occurs after stack full becomes valid but before the jump conditions are tested.

Control panel interrupt logic is also factored into the interrupt request. Once the microprogram recognizes an interrupt, it tests the CPINT jump condition to determine if it is a general interrupt or a control panel interrupt. For a general interrupt, it performs a JSR to location 0001. For a control panel interrupt, the microprogram pulses the CPINP control flag which indicates that an instruction should be jammed in by the control panel logic. In this system, CPINP clears the address register and requests a memory read cycle. The net effect is that the instruction at location 0000 is executed out of normal sequence. This instruction could be virtually anything (JSR @ is prohibited for some unknown reason). Typically, a JSR to the monitor is used. The debouncer and synchronizer needed for direct connection of a SPDT switch to the edge connector is included.

Figure 7 shows the data register. As with the address register, it is clocked every microcycle by CPU LOAD REG. It is enabled to receive data only if the WRM (write memory) control flag is on. The tristate outputs are enabled during CPU write cycles when BUS DATA IN ENAB is active. The status flag latch which is strictly a convenience feature is also shown on this page.

Figure 8 shows the CPU transceivers and jump/flag address latch. The transceivers normally receive data from the PMOS RALU data bus. They are switched to transmit mode when CPU DATA IN ENAB is active. The flag address latch is clocked by CPU FLAG ADDR STB and should be of the transparent variety such as a 7475 to insure minimum through delay.

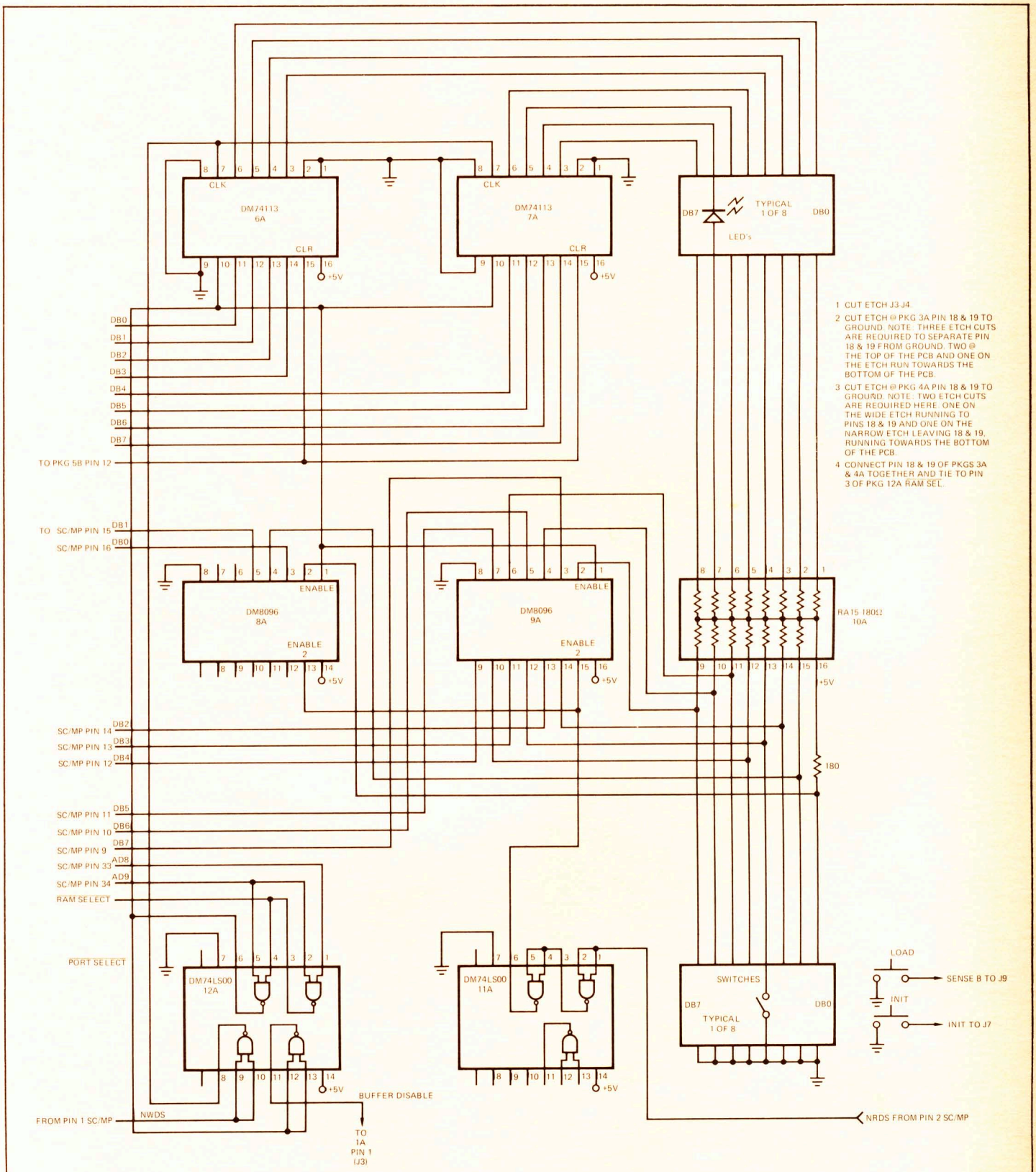
A couple of guidelines should be noted by those who wire-wrap their CPU cards. First, the IC's that tie to the PUNIBUS should be as close as possible to the corresponding edge fingers. This applies to other cards in the system as well. Second, the clock drivers should be right next to the IMP chips which should in turn be close to each other. The +5 and −12 supply voltages for these chips should be bypassed right at the power connections for each chip. Keep the crystal oscillator and timing ROM's compact also.

Debugging the CPU card after construction is normally not difficult however a dual trace scope with at least 15 mHz bandwidth is required. First, plug in all of the IC's associated

(continued on page 11)

SCRIMP.... WITH SC/MP!

If you've got to scrimp a little on your SC/MP system, here's the way to do it. Shown below are the instructions, listings, block diagrams, schematic diagrams, and wiring diagrams for "SCRIMP" an on-board terminal for the SC/MP kit. SCRIMP eliminates the need for a Teletype, so if you don't have one hanging around, you might want to build this circuit. If you run into any difficulty, you can contact Dan Grove at the Santa Clara Training Center, or Hugh Kelly, Dallas, Texas (214) 690-4195.


DM74113 6A
DM74113 7A
CLK
CLR
+5V
TYPICAL 1 OF 8
DB7
DB0
LED's
1 CUT ETCH J3 J4.
2 CUT ETCH @ PKG 3A PIN 18 & 19 TO GROUND. NOTE: THREE ETCH CUTS ARE REQUIRED TO SEPARATE PIN 18 & 19 FROM GROUND. TWO @ THE TOP OF THE PCB AND ONE ON THE ETCH RUN TOWARDS THE BOTTOM OF THE PCB.
3 CUT ETCH @ PKG 4A PIN 18 & 19 TO GROUND. NOTE: TWO ETCH CUTS ARE REQUIRED HERE. ONE ON THE WIDE ETCH RUNNING TO PINS 18 & 19 AND ONE ON THE NARROW ETCH LEAVING 18 & 19, RUNNING TOWARDS THE BOTTOM OF THE PCB.
4 CONNECT PIN 18 & 19 OF PKGS 3A & 4A TOGETHER AND TIE TO PIN 3 OF PKG 12A RAM SEL.
TO PKG 5B PIN 12
TO SC/MP PIN 15
SC/MP PIN 16
DM8096 8A
DM8096 9A
ENABLE
ENABLE 2
RA15 180Ω 10A
180
SC/MP PIN 14
SC/MP PIN 13
SC/MP PIN 12
SC/MP PIN 11
SC/MP PIN 10
SC/MP PIN 9
SC/MP PIN 33
SC/MP PIN 34
RAM SELECT
PORT SELECT
DM74LS00 12A
DM74LS00 11A
BUFFER DISABLE
FROM PIN 1 SC/MP
NWDS
TO 1A PIN 1 (J3)
SWITCHES
LOAD
SENSE B TO J9
INIT
INIT TO J7
NRDS FROM PIN 2 SC/MP

SCRIMP SCHEMATIC DIAGRAM

SC/MP
LOW COST
DEVELOPMENT SYSTEM

National Semiconductor

SC/MP Low Cost Development System

The SC/MP Low Cost Development System (LCDS) is a simple controller configured to provide maximum flexibility at affordable cost. It provides all the features necessary for development and testing of SC/MP hardware and software designs for a user's applications.

The minimum SC/MP Development System is configured with a SC/MP CPU Card plugged into one of four sockets in a Card Bus on a 10" x 12" motherboard. Also on the motherboard are a 16 key, dual-function, hexidecimal keyboard; four function keys; 3 control switches and a 6 digit hexidecimal display.

Control logic, scratchpad memory, and ROM based firmware on the motherboard allow the user to examine and alter the SC/MP registers, examine and alter memory locations, run SC/MP programs in continuous or single instruction mode or operate with an optional Teletype® using SC/MP DEBUG.

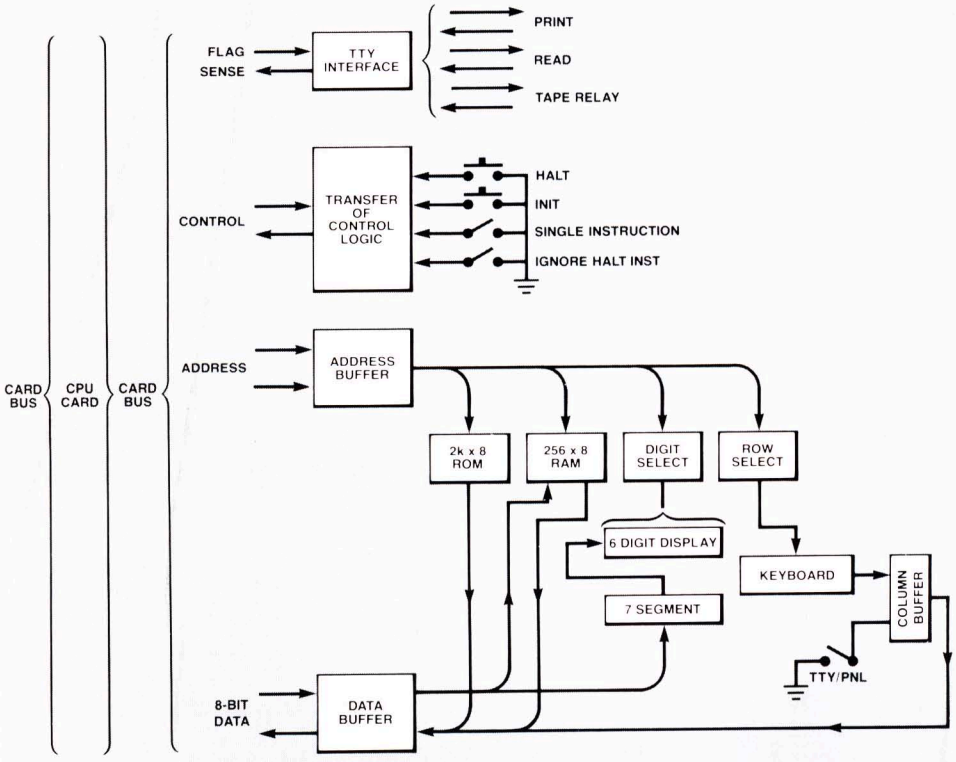


Figure 1: BLOCK DIAGRAM FOR MOTHERBOARD

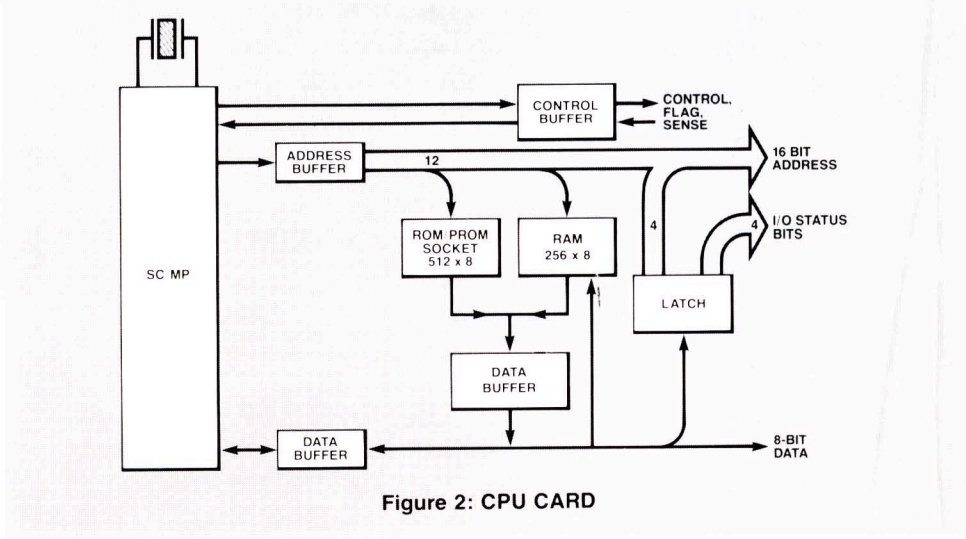


Figure 2: CPU CARD

FEATURES

Salient operating characteristics of the major items comprising the LCDS are as follows.

SC/MP CPU Card

The basic block diagram of the SC/MP CPU card (ISP-8C/100) is shown in Fig. 2. It provides the CPU interface for execution of user-generated application programs and development system resident firmware.

Pre-wired Application System Interface

Four prewired 72-pin edge connector sockets provide a plug-in interface for SC/MP family cards and permit interconnection of additional SC/MP applications hardware via user fabricated cabling. A fifth 72-pin edge connector can be added by the user. In addition, a flat cable connector can be added for coupling to an external card cage.

Interface Logic

Provides control and monitor functions that permit transfer of control between development system resident firmware and user-generated application programs.

Development System Resident Firmware Program

This firmware contains subroutines that permit entry of software debug commands via the programmer's control and display panel, or an optional Teletype.

Programmer's Control and Display Panel

Provides the following software debug capabilities:

- **Display contents of SC/MP program counter, registers, and accumulator in hexadecimal format.**
- **Alter contents of SC/MP program counter, registers and accumulator.**
- **Display contents of any memory location in hexadecimal format.**
- **Alter contents of any memory location.**
- **Initiate execution of user-generated application program at any memory address.**
- **Select single instruction or normal execution of user generated application program.**
- **Interrupt execution of user-generated application program at any point.**

Teletype Interface-

Provides standard 20-milliampere interface for interconnection of optional Teletype. Expanded software debug capabilities associated with Teletype option include:

- **Print contents of SC/MP program counter, registers, and accumulator**
- **Alter contents of SC/MP program counter, registers, and accumulator**

  Print contents of any single memory location or selected range of memory locations
- **Alter contents of any memory location or selected range of memory locations**
- **Set a breakpoint halt in RAM for user-generated application program**
- **Initiate execution of user-generated application program at any memory address**
- **Save application program by punching selected memory range to paper tape**
- **Load development system generated paper tape into memory**
- **Load IMP-16 or FORTRAN Cross Assembler generated paper tape into memory.**

Expanding the SC/MP Low Cost Development System

National Semiconductor offers various cards which may be used in conjunction with the SC/MP LCDS System. The 2K x 8 Read/Write Memory Card (ISP-8C/002) and the 4K x 8 ROM/PROM Card (ISP-8C/004) can be used to provide additional memory for user application or system development.

The standard Cards can be plugged into any of the connectors on the Card Bus. The bus is easily expanded by use of flat-cable to external user supplied modules.

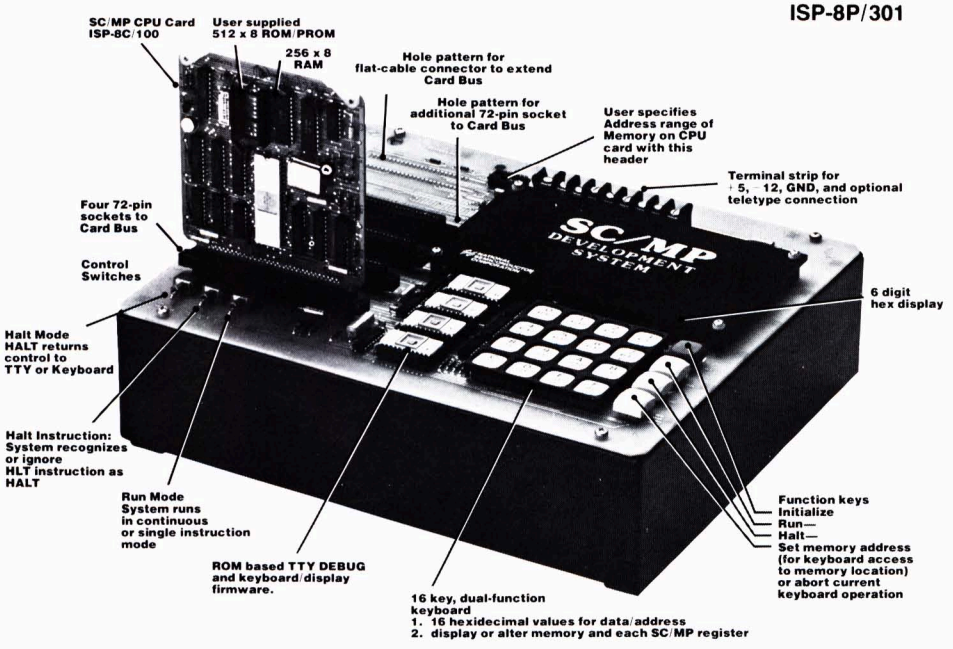
Typical use of the system provides capability to debug user systems with program in RAM, using features of DEBUG such as single instruction or breakpoints. Changes to the program can be made directly from the keyboard or teletype. When the program is running correctly, it can be dumped to paper tape for programming ROM or PROM.

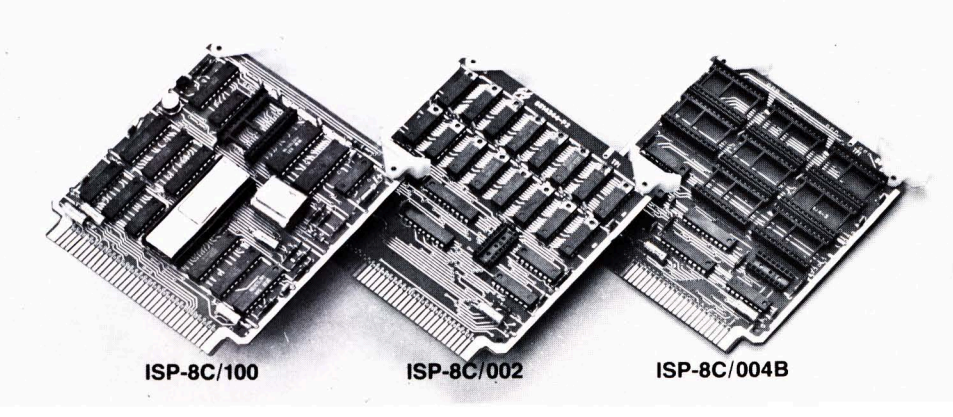
Ordering Information

The SC/MP LCDS and supporting cards may be ordered directly from National Semiconductor or National's franchised distributor near you.

SC/MP LCDS (includes one CPU Card)	**ISP-8P/301**
SC/MP RAM Card (2K x 8)	**ISP-8C/002**
SC/MP ROM/PROM Card (4K x 8) (includes eight 5204 PROMs)	**ISP-8C/004P**
SC/MP ROM/PROM Card (4K x 8) (without PROM Memory)	**ISP-8C/004B**
SC/MP CPU Card	**ISP-8C/100**

ISP-8P/301


SC/MP CPU Card ISP-8C/100
User supplied 512 x 8 ROM/PROM
256 x 8 RAM
Hole pattern for flat-cable connector to extend Card Bus
Hole pattern for additional 72-pin socket to Card Bus
User specifies Address range of Memory on CPU card with this header
Terminal strip for +5, 12, GND, and optional teletype connection
Four 72-pin sockets to Card Bus
Control Switches
6 digit hex display
Halt Mode HALT returns control to TTY or Keyboard
Halt Instruction: System recognizes or ignore HLT instruction as HALT
Run Mode System runs in continuous or single instruction mode
ROM based TTY DEBUG and keyboard/display firmware.
16 key, dual-function keyboard
1. 16 hexidecimal values for data/address
2. display or alter memory and each SC/MP register
Function keys
Initialize
Run
Halt
Set memory address (for keyboard access to memory location) or abort current keyboard operation
SC/MP DEVELOPMENT SYSTEM



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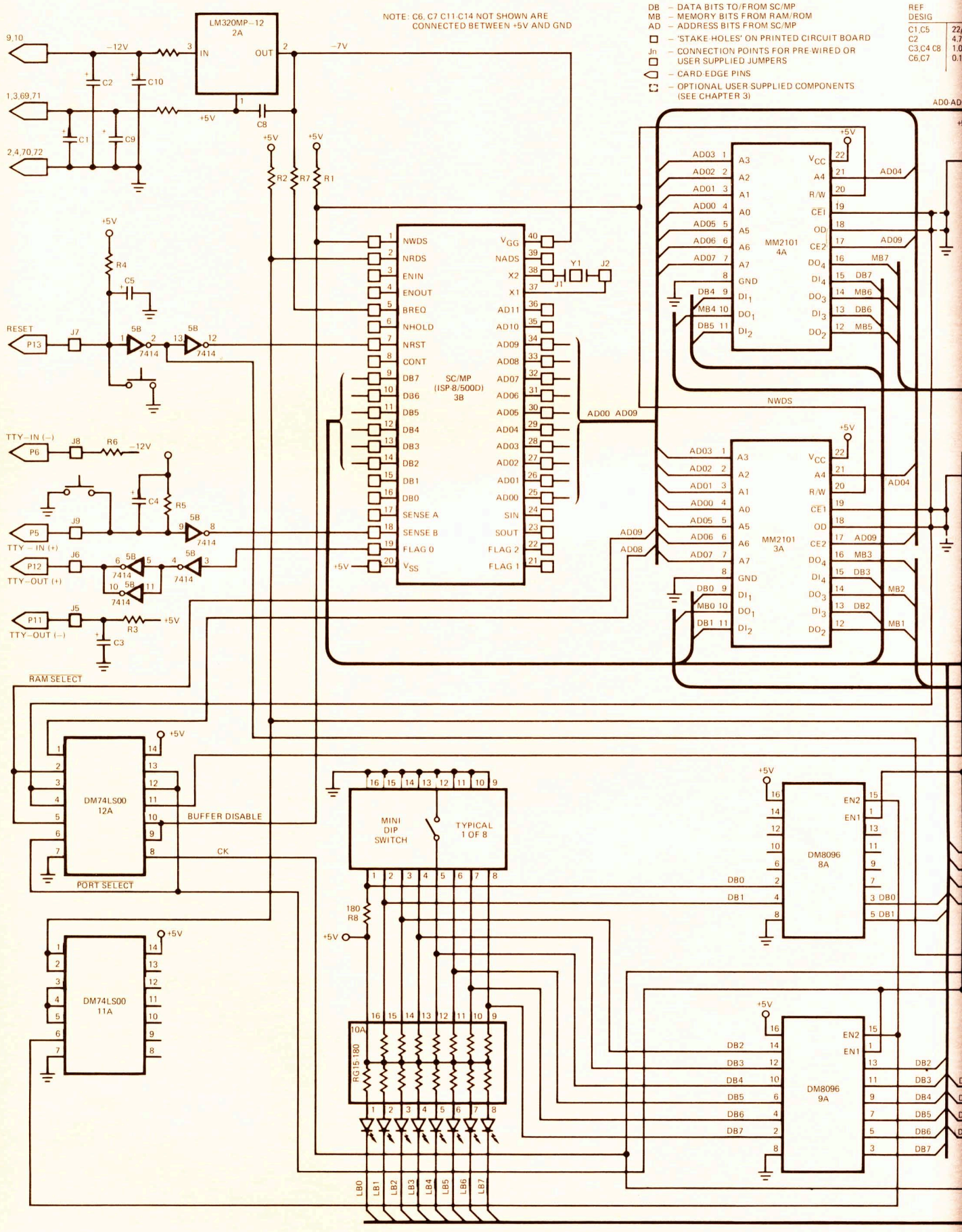
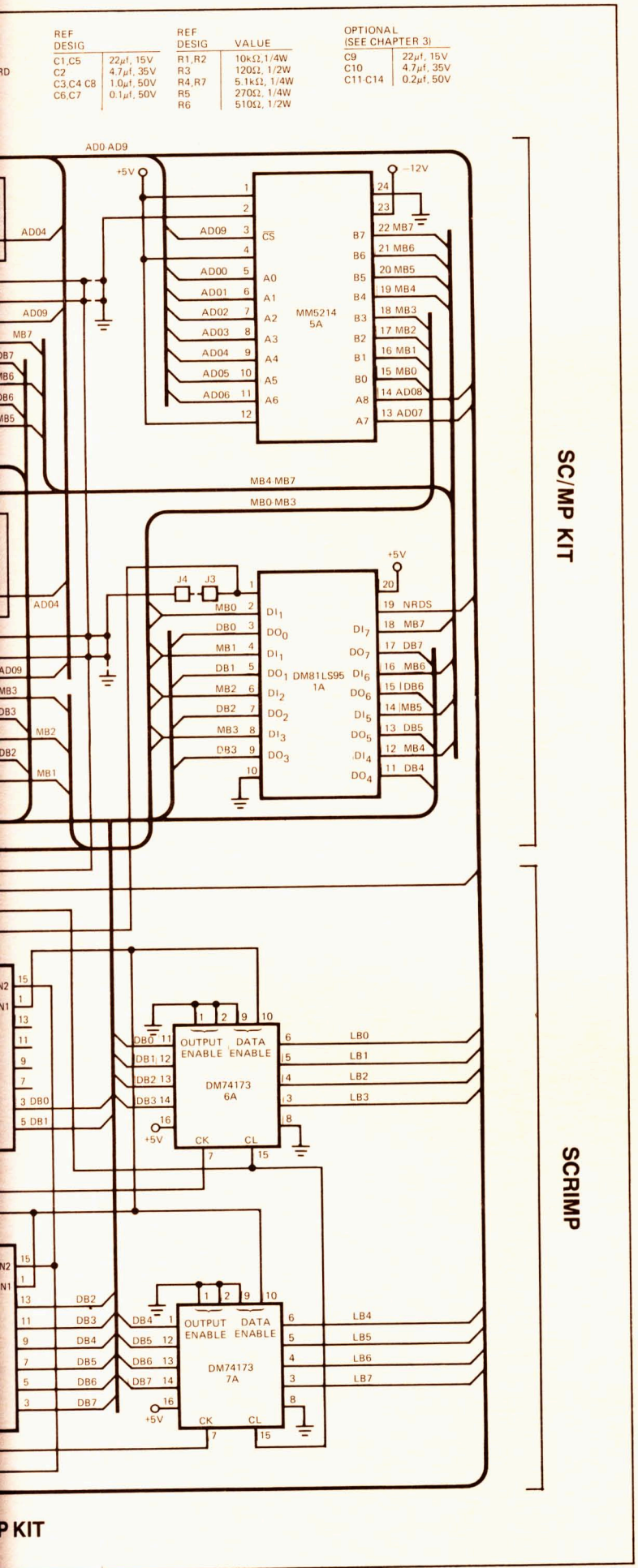


COMPLETE SCHEMATIC DIAGRAM INCLUDING SC/MP KIT



SCRIMP INSTRUCTIONS

SCRIMP utilizes the KITBUG program in the SC/MP microprocessor evaluation kit. Refer to the SC/MP kit Users Manual (Ch. 4—Using KITBUG) for a detailed description of the KITBUG operation.

T = "Type" in KITBUG = "Read in SCRIMP = 01
M = "Modify" in KITBUG = "Write" in SCRIMP = 02
G = "Go" in KITBUG = "Run" in SCRIMP = 04

SCRIMP prompt is all lights on (FF)

EXAMPLES: 1. "Read" Mode:

	Operator Action	Display
Push	INIT	FF (prompt)
Enter	01 in data switches (Read Code)	
Push	Load Data	01 (acknowledge)
Enter	high byte of address A in data switches (aa_H)	
Push	Load Data	aa_H (acknowledge)
Enter	low byte of address A in data switches (aa_L)	
Push	Load Data (read data in A)	dd_A (data)
Push	Load Data (read data in A+1)	dd_{A+1} (data)

2. "Write" Mode

Push	INIT	FF (prompt)
Enter	02 in data switches (write code)	
Push	Load Data	02 (acknowledge)
Enter	high byte of address A in data switches (aa_H)	
Push	Load Data	aa_H (acknowledge)
Enter	low byte of address A in data switches (aa_L)	
Push	Load Data (read data in A)	dd_A (data at A)
Enter	data (d'd'$_A$)	
Push	Load Data (write d'd'$_A$ in A)	dd_{A+1} (data at A+1)

NOTE: If you wish to alter the next location without modifying the present location, you must re-enter the data at the present location so that it is not accidentally changed.

3. "Run" Mode

Push	INIT Establish PC start address as in KITBUG:	FF (prompt)
Enter	02 in data switches (write code)	
Push	Load Data	02 (acknowledge)
Enter	high byte of PC initialize address in data switches (0F)	
Push	Load Data	0F (acknowledge)
Enter	low byte of PC initialize address in data switches (F7)	
Push	Load Data (read data in 0FF7)	pp_H (data in 0FF7)
Enter	high byte of PC in data switches (p'p'$_H$)	
Push	Load Data (write p'p'$_H$ in 0FF7)	pp_L (data in 0FF8)
Enter	low byte of PC in data switches (p'p'$_L$)	
Push	Load Data (write p'p'$_L$ in 0FF8)	pp_9 (data in 0FF9)
Push	INIT	FF
Enter	04 in data switches (run code)	
Push	Load Data	04 (acknowledge)
Push	Load Data = Runs Program	

Registers in top locations of RAM utilized by executive program:

0FF5	Current Command Code
0FF6	Address Completion Flags
00F7	High byte of PC
0FF8	Low byte of PC
0FF9	High byte of P1
0FFA	Low byte of P1
0FFB	High byte of P2
0FFC	Low byte of P2
0FFD	Accumulator
0FFE	Extension Register
0FFF	Status Register

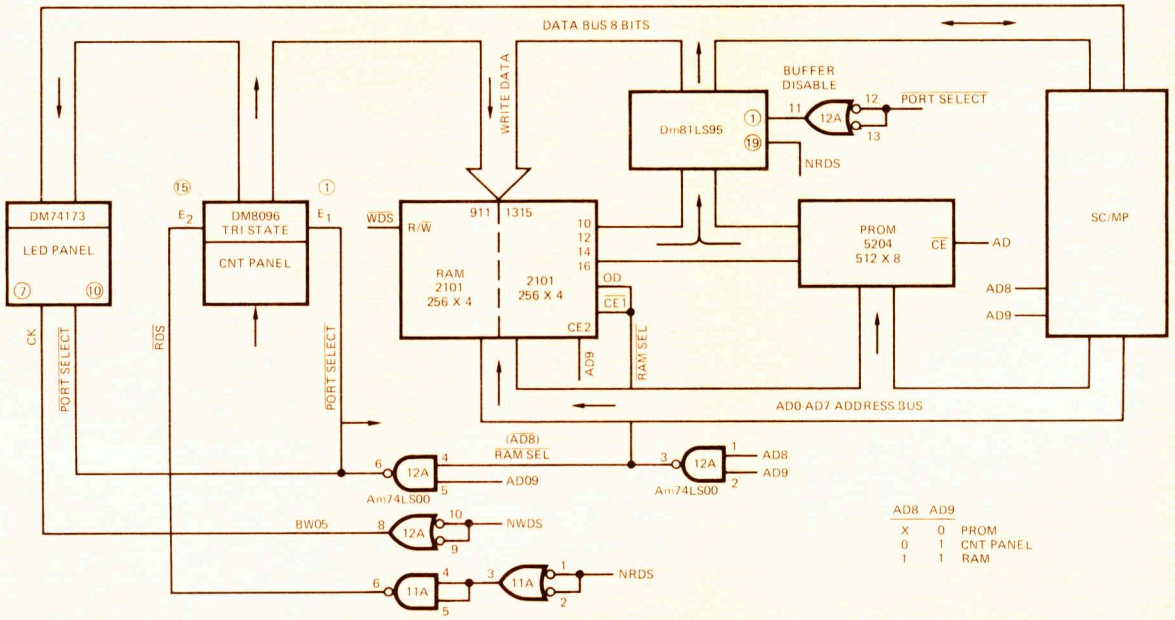
(continued on next page)

SCRIMP WITH SC/MP, continued

```
                        TITLE SCRIMP,' SC/MP KIT TERMINAL'

                        05/18/76



0020                    SE=020
0080                    LINK=080

0001                    RFLAG=1
0002                    WFLAG=2
0004                    GOFLAG=4

                        FIXED STACK ASSIGNMENTS

0FFF                    .=0FFF

                STACK:
0000            SR=.-STACK
0FFE                    .=.-1
FFFF            EX=.-STACK
0FFD                    .=.-1
FFFE            AC=.-STACK
0FFB                    .=.-2
FFFC            PT2=.-STACK
0FF9                    .=.-2
FFFA            PT1=.-STACK
0FF7                    .=.-2
FFF8            PC=.-STACK
0FF6                    .=.-1
FFF7            ADR=.-STACK
0FF5                    .=.-1
FFF6            CMD=.-STACK

                        .PAGE

0000                    .=0

0000 08                 NOP
0001 903B               JMP    CMDLP

                DEBUG EXIT-RESTORE ENVIRONMENT AND GO

0003 C0FA  EXIT:        LD     STACK+EX        ;RESTORE E REG
0005 01                 XAE
0006 C0F2               LD     STACK+PT1
0008 35                 XPAH   1
0009 C0F0               LD     STACK+PT1+1
000B 31                 XPAL   1
000C C0EE               LD     STACK+PT2
000E 36                 XPAH   2
000F C0EC               LD     STACK+PT2+1
0011 32                 XPAL   2
0012 C0E4               LD     STACK+PC
0014 37                 XPAH   3
0015 C0E2               LD     STACK+PC+1
0017 33                 XPAL   3
0018 C7FF               LD     @-1(3)          ;ADD EXIT OFFSET
                                                TO PC
001A C0E4               LD     STACK+SR
0010 07                 CAS
001D C0DF               LD     STACK+AC
001F 3F                 XPPC   3
0020 9002               JMP    ENTER
0022 90DF  EXITP:       JMP    EXIT

                DEBUG ENTRY POINT

0024 C8D8  ENTER:       ST     STACK+AC
0026 06                 CSA
0027 C8D7               ST     STACK+SR
0029 01                 XAE
002A C8D3               ST     STACK+EX
002C 36                 XPAH   2
002D C8CD               ST     STACK+PT2
002F 32                 XPAL   2
0030 C8CE               ST     STACK+PT2+1
0032 35                 XPAH   1
0033 C8C5               ST     STACK+PT1
0035 31                 XPAL   1
0036 C8C3               ST     STACK+PT1+1
0038 37                 XPAH   3
0039 C8EB               ST     STACK+PC
003B 33                 XPAL   3
003C C8BB               ST     STACK+PC+1

                        .PAGE
                INITIALIZE AND AWAIT COMMAND ENTRY

003E C40F  CMDLP:       LDI    0F              ;PUT STACK
                                                BASE ADRS
0040 35                 XPAH   1               ; IN P REG 1
0041 C4FF               LDI    0FF
0043 31                 XPAL   1
0044 C402               LDI    02              ;PUT DEVICE ADRS
0046 36                 XPAH   2               ;IN P REG 2
0047 C400               LDI    0
0049 32                 XPAL   2
004A C400  BADCMD:      LDI    0
004C C9F6               ST     CMD(1)          ;INIT FLAGS
004E C9F7               ST     ADR(1)
0050 CA00               ST     (2)             ;DISPLAY OFF

0052 06    TEST:        CSA                    ;WAIT FOR
                                                COMMAND ENTRY
0053 D420               ANI    SB
0055 98FB               JZ     TEST
0057 8F3C               DLY    60              ;DEBOUNCE 60 MS.
0059 06    WAIT:        CSA
005A D420               ANI    SB
005C 9CFB               JNZ    WAIT
005E 8F3C               DLY    60              ;DEBOUNCE 60 MS.

0060 C1F6               LD     CMD(1)          ;COMMAND ALREADY
                                                RECEIVED?
0062 9C36               JNZ    CHEKA1          ;YES
0064 C200               LD     (2)             ;NO-MUST BE A
                                                NEW COMMAND
0066 1F                 RRL                    ;SEE WHAT IT IS
0067 01                 XAE                    ;SAVE REST OF
                                                COMMAND WORD
0068 06                 CSA
0069 D480               ANI    LINK
006B 9CIF               JNZ    READ
006D 40                 LDE
006E 1F                 RRL
006F 01                 XAE
0070 06                 CSA
0071 D480               ANI    LINK
0073 9C1E               JNZ    WRITE
0075 40                 LDE
0076 1F                 RRL
0077 01                 XAE
0078 06                 CSA
0079 D480               ANI    LINK
007B 98CD               JZ     BADCMD          ;INVALID COMMAND

007D 40                 LDE                    ;GET REST OF
                                                COMMAND WORD
007E 9CCA               JNZ    BADCMD          ;INVALID COMMAND
0080 C404               LDI    04
0082 C9F6  SETCMD:      ST     CMD(1)          ;SET GO FLAG
0084 E4FF               XRI    0FF             ;DISPLAY COMMAND
0086 CA00               ST     (2)
0088 90C8  TESTP:       JMP    TEST

008A 9696  EXITP1:      JMP    EXITP
008C 40    READ:        LDE
008D 9CBB               JNZ    BADCMD          ;INVALID COMMAND
008F C401               LDI    01
0091 90EF               JMP    SETCMD)

0093 40    WRITE:       LDE
0094 9CB4               JNZ    BADCMD          ;INVALID COMMAND
0096 C402               LDI    02
0098 90E8               JMP    SETCMD

009A C1F6  CHEKA1:      LD     CMD(1)          ;IS THIS GO
                                                COMMAND?
009C D404               ANI    GOFLAG
```

SCRIMP WITH SC/MP, continued

```
152  009E 9C21            JNZ   GOCMD      ;YES
153
154  00A0 C1F7            LD    ADR(1)     ;IS THIS 1ST
                                             ADR BYTE?
155  00A2 9C0F            JNZ   CHEKA2     ;NO
156  00A4 C200            LD    (2)        ;YES-GET IT
157  00A6 E4FF            XRI   0FF
158  00AS CA00            ST    (2)        ;DISPLAY IT
159  00AA E4FF            XRI   0FF
160  00AC 37              XPAH  3
161  00AD C401            LDI   01         ;SET 1ST
                                             BYTE RECEIVED
162  00AF C9F7            ST    ADR(1)
163  00B1 909F            JMP   TEST
164
165  00B3 02    CHEKA2:   CCL
166  00B4 F4FF            ADI   -1
167  00B6 9C0F            JNZ   ADDONE     ;IS THIS 2ND
                                             ADR BYTE?
168  00BS C200            LD    (2)        ;YES-GET IT
169  00BA 33              XPAL  3
170  00BB C402            LDI   02
171  00BD C9F7            ST    ADR(1)
172  00BF 900C            JMP   S1
173
174  00C1 C4FF  GOCMD:    LDI   0FF        ;TURN OFF DISPLAY
175  00C3 CA00            ST    (2)
176  00C5 90C3            JMP   EXITP1
177
178  00C7 C1F6  ADDONE:   LD    CMD(1)     ;ADDRESS COMPLETE
179  00C9 D401            ANI   RFLAG      ;READING OR
                                             WRITING?
180  00CB 9808            JZ    S2         ;WRITING
181  00CD C701  S1:       LD    C1(3)
182  00CF E4FF            XRI   0FF
183  00D1 CA00            ST    (2)
184  00D3 90B3            JMP   TESTP
185
186  00D5 C200  S2:       LD    (2)
187  00D7 CBFF            ST    -1(3)
188  00D9 90F2            JMP   S1
189
190       0000            .END
```



BLOCK DIAGRAM

WESTERN TRAINING CENTER IS ON THE MOVE!

National Semiconductor has moved its Western Microprocessor Training Center to custom designed facilities in Suite 430 at Marina Playa, 1333 Lawrence Expressway, Santa Clara, CA 95051. Marina Playa is a beautiful new office complex within walking distance of several excellent motels and restaurants. The move makes our center more convenient for all students, but especially for the out of town students. Now you don't have to spend a lot of time traveling from a motel or restaurant to the center. Instead, you can spend the time in front of a microprocessor, and after all, isn't that the reason why you go to a microprocessor training class? And speaking of equipment, at the Western Training Center you get your own personal microprocessor system for as much hands-on experience as you want.

And if that wasn't enough, you get the finest staff of instructors in the microprocessor field: Bill Harding and Dan Grove on hardware and Georgia Marszalek (our own Georgia) on software. To go into the background qualifications of the staff would take up half of the newsletter. So, I will just say, if you want to learn microprocessors, and have a great time (San Francisco is just up the road), go west, to your Western Training Center.

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Georgia Marszalek at
(408) 247-7924
or
Bill Harding at
(408) 737-6453

with the bus controller as well as the two 8334 control flag registers. Check for proper functioning of the POWER OK and BUS RESET lines. Next check the bus controller timing signals. It should be executing read cycles and granting these to the refresh logic. If the timing generator seems to be stuck, check for wiring errors or a bad 74S174 or timing PROM. The write timing signals may be checked by temporarily grounding BUS WRITE CYCLE REQ. Check also for lengthening of BUS CE by about 50Ns during write cycles. Verify that the refresh counter is incrementing every bus cycle and that the count is gated onto the bus data lines at the proper time.

Before continuing, check the supply voltage to the clock driver sockets for proper polarity, magnitude, and pin numbers. Now plug in the remaining TTL chips but not the IMP chips. The bus controller should function as before. Check the clock driver outputs. Some ringing is normal on the unloaded clock lines. Check every pin of every IMP chip socket for reasonable voltage levels. Be careful not to short clock lines together or to anything else.

Now plug in the IMP chips and blank (all ZEROS) IPL ROM's. After reset the HALT flag should be set by the microprogram since a HALT will be fetched from the blank ROM at location FFFE. Two depressions of the START button should turn HALT off for a fraction of a second (no memory or I/O plugged into the system) while FFFF (a skip if not equal instruction which will in all likelihood skip) is fetched from the nonexistent memory. If this works, the CPU is at least 80% functional.

So, what if it doesn't work? About the only way to tell what the microprogram is doing is to examine the jump/flag addresses it is sending out along with the NFLEN signal. A good initial troubleshooting method is to drive the BUS POWER OK line on and off at about a 10Hz rate and sync the scope on the

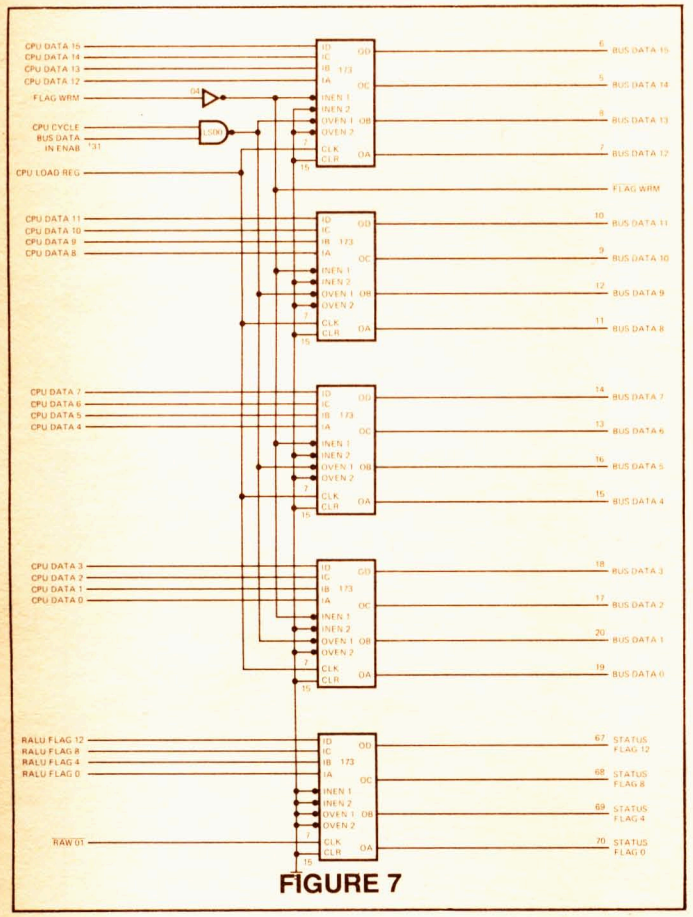


FIGURE 7

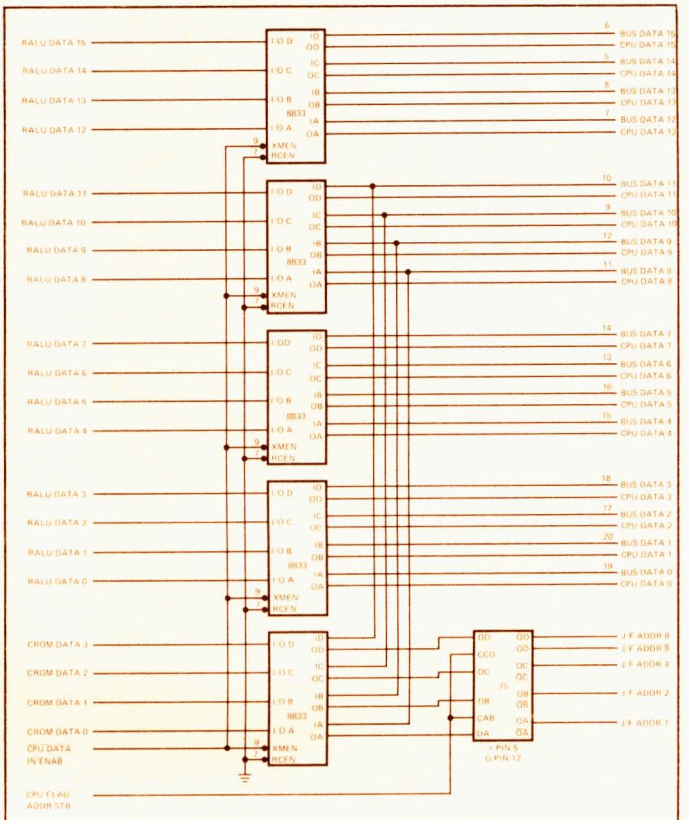


FIGURE 8

4-phase decoder enable flop. Then the sequence of events after reset can be viewed fairly easily. The microprogram should first pulse the RDM (read memory) flag and load FFFE into the address register. A bus cycle should be granted to the CPU and all ZEROES should be gated into the CPU during T7. The microprogram should respond by setting the HALT flag and then entering a loop testing the START jump condition. A break in this chain may send the CPU off wildly or even halt the microprogram if an illegal op-code is encountered.

If you think your chip set is substandard, temporarily substitute a crystal in the 10 to 13 mHz range. If this straightens things out or even makes a difference, leave it there until the system is up and some diagnostics can be run to determine the speed limit for your chip set.

In part 4, the memory board and some notes on I/O interfacing will covered. Additionally, more detailed information on getting the system up and running will be given.

APPENDIX JUMP CONDITION ASSIGNMENT

0 Interrupt request (general or control panel)
1 Result equals zero
2 Result not negative
3 Bit 0 of result is a ONE
4 Bit 1 of result is a ONE
5 Result is not zero
6 Control panel interrupt request
7 Start switch is depressed
8 The on-chip stack is full (bottom word is non-zero)
9 The interrupt enable control flag is on
A The carry/overflow line is a ONE
B Result is not positive
C The carry/overflow line is a ZERO
D Result is positive
E Result is negative
F Bit 2 of result is a ONE

APPLICATIONS CORNER:

High Performance, Low Power Memories from Inexpensive Parts!

You can use standard, inexpensive, bipolar PROMS to build high-performance memories of low power dissipation. The secret is to power-down the chip when it is not being accessed.

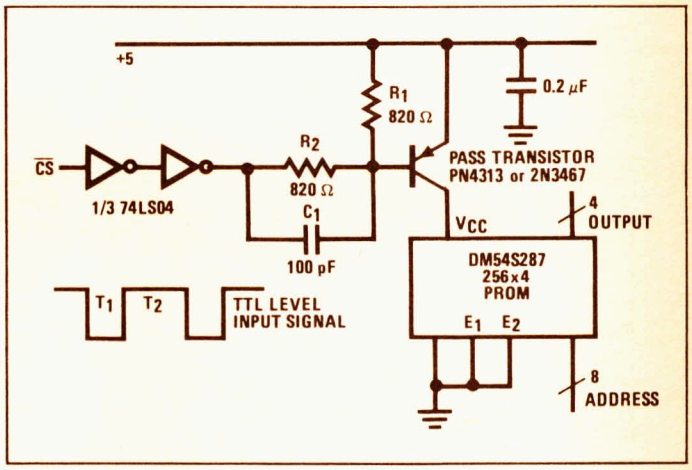
The technique illustrated here results in a power savings beyond that possible with bipolar PROMS having on-chip power-down, and the cost is much less than that of CMOS PROMS of the same capacity. In fact, because the access time of the circuit shown here is less than 80 ns, the power savings can be greater than 10 to 1 if the circuit is cycled every microsecond. Longer cycle times, or decoding of the power switching to multiple packages, yields even more impressive ratios.

National's PROMS are well behaved in this application. With power removed, our Tri-State® parts revert quickly to their third state (a high-impedance open). Because there are no clamp diodes from the outputs to V_{CC}, the powered-down device presents only leakage to the output bus.

Note that in a CMOS system, passive pull-ups are desirable to establish the CMOS input level at V_{CC} when the PROM is powered down. If the CMOS input is more than a threshold away from both supply rails, the input stage of the CMOS device may draw supply current, which will increase system power dissipation. Here it is desirable to clock the PROM outputs directly into a CMOS holding register to reduce the time that the PROM must be powered up. Also, the pnp core driver pass elements can be driven directly by an MM74C42 1-of-10 decoder output without pull-up or current limiting resistors, with some increase in effective access time.

The MM74C42 would replace the 74LS04 shown here.

In any system that switches a device's supply lead to conserve power, the power supply bypassing must be performed on the supply side of the power switch; that is, at the pnp emitter. Any capacitance at the collector of the pnp will increase both system power dissipation and access time.



the Bit-Bucket

Sirs:

I am interested in knowing if you have in your library of programs a program for interfacing the SC/MP to a 5 level TTY machine.

The older style machine is a Western Union Teleprinter, Mod. #105.

The word rate of this machine is 60 words per min.

I would like the program to include a SC/MP debug program and a teletype load, and print routines.

I would also like to know if this program is available in a ROM that can be exchanged for the normal 8 level TTY, debug program of the SC/MP kit.

If not, I would like the cost of a pre-punched 8 level tape for loading my PROMs from my PROM loader.

If the program is not available I would like some program ideas on setting up a TTY load program.

Your attention on these matters will be appreciated.

Sincerely
H. Mattice
1375 Langly Dr.
Gardnerville, Nevada 89410

The program you are looking for is not part of our user library. If any users have written a program to interface the SC/MP Kit to a 5 level TTY, please let us know of your efforts. To write the program one would have to do the ASCII decoding for the 5 levels and change the software delays in the TTY interface routine for the SC/MP Kit. See the Kit Bug listing in the SC/MP Kit manual for a start.

Dear Georgia:

Received calculator in working order in spite of the U.S. mule hoof marks on the carton. Thank you.

In a few weeks I hope to have a universal program for debugging PACE application systems. One PACE application PROM card will provide a simple DEBUG routine which will accept a very limited, coded word input from a TTY keyboard, 5 hex characters, to enable a tester to address any input or output address in any system. By turning on certain outputs and observing the results or reading corresponding inputs, every wire and switch in the application system can be verified. This should be of interest to PACE users.

Very truly yours,

Walter L. Probert
Senior Development Engineer

the Bit-Bucket, continued

Walt received one of the calculators offered for contributions to the newsletters.

Georgia Marszalek, Compute Ins,

Dear Georgia:

Just received some new listings for GENLDR and IMPASM. I notice they are assembled using Rev H of the Assembler which includes new directives like .PTR, .POOL, .NOBAS etc.

Is there any publication which defines the changes to get from Rev. G to Rev. H without having to procure a new card deck.

Henry J. Lyons, P.E.
6901 100th Ave.
Seabrook, Md. 20801

The directives you found in your source listing are only found in the FORTRAN Cross Assembler for PACE and IMP-16. These are used by National's programming staff to develop software. There is no document that describes their use because they are not currently supported in the resident assemblers. Also no document has been published that details the changes between Rev. G and Rev. H of the FORTRAN Cross Assembler for IMP-16.

Dear Ms. Marszalek

Three requests please:

1. Please send me a listing of user library SL0027A SC/MP Math Package.
2. Will National (or someone) be selling a ROM containing the cassette recorder program in AN-163?
3. Are back issues of COMPUTE available? Is there a charge?

Sincerely,
Ronald G. Parsons
9001 Laurel Grove Drive
Austin, Texas 78758

Under separate cover I have sent a copy of the SC/MP math routines.

Right now there are no plans to sell a ROM containing the cassette recorder program. But the source and/or object tapes can be purchased from the user library for $5.00 each by ordering SL0039A.

Some back issues of COMPUTE are available. Which ones would you like?

Gentlemen:

I have known about your work through a publication named "SC/MP Technical Description", and I am very interested in getting in touch with you.

I am working in some projects that involve microprocessors, and for the uses for which I plan to use them, the SC/MP is the best one, but here, in Uruguay, it is quite difficult to obtain technical information concerning microprocessors. Would you please be so kind in sending me a membership application and detailed information about Compute.

Thanking you in advance and waiting for your news at your early convenience.

Yours sincerely,
Washington Varela
Luis M. Lafinur Nº 2131
Montevideo—Uruguay

They write to us from far and near.

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